CLAIMS

1. An apparatus comprising:

one or more groups of boundary scan cells;

one or more group buffers coupled to each of said groups of boundary scan cells;

one or more repeater buffers coupled in series with said group buffers; and

a controller coupled to said groups of boundary scan cells through said group buffers and said repeater buffers, wherein said apparatus is configured to buffer said groups of boundary scan cells to reflect an order of I/Os around said apparatus.

2. The apparatus according to claim 1, wherein said groups of boundary scan cells comprise a scan chain.

3. The apparatus according to claim 2, wherein said repeater buffers are configured to eliminate skew at the beginning pins and end pins of the scan chain.

4. The apparatus according to claim 1, wherein said apparatus further comprises:

one or more boundary scan control nets configured to control said groups of boundary scan cells.

5. The apparatus according to claim 1, wherein said apparatus is configured to route said groups of boundary scan cells in an I/O portion of said apparatus.

6. The apparatus according to claim 1, wherein each boundary scan cell of said groups of boundary scan cells are implemented within an I/O cell.

7. The apparatus according to claim 1, wherein said apparatus comprises a clock chain in a first direction and a data path in an opposite direction of said first direction.

8. The apparatus according to claim 1, wherein a scan connection of apparatus is controlled by a scan enable signal.

9. The apparatus according to claim 1, wherein said apparatus implements one or more flip flips, each configured to provide a scan enable output.

10. An apparatus comprising:

means for implementing one or more groups of boundary scan cells;

means for implementing one or more group buffers coupled to each one of said groups of boundary scan cells;

means for implementing one or more repeater buffers coupled in series with said group buffers; and

means for controlling coupled to said groups of boundary scan cells through said group buffers and said repeater buffers; and

means for buffering said groups of boundary scan cells to reflect an order of I/Os around said apparatus.

11. A method for optimizing buffers for JTAG boundary scan nets, comprising the steps of:

(A) reading a netlist;

(B) reading an I/O order list;

(C) defining a number of I/Os per groups;

(D) determining if a last I/O is connected; and

(E) writing a final netlist.

12. The method according to claim 11, wherein step (D) further comprises:

determining if starting a new group is necessary.

13. The method according to claim 12, wherein step (D) further comprises:

splitting a net.

14. The method according to claim 13, wherein step (D) further comprises:

inserting a repeater buffer.

15. The method according to claim 14, wherein step (D) further comprises:

inserting a group buffer.

16. The method according to claim 12, wherein step (D) further comprises:

connecting a next I/O a newest group buffer.

17. The method according to claim 11, further comprising the following step:

repeating step (D).

18. The method according to claim 11, wherein step (E) further comprises:

buffering said JTAG boundary scan nets to reflect the order of I/O cells around a circuit.

19. The method according to claim 11, wherein steps (E) further comprises:

providing boundary scan cell placement.

20. The method according to claim 11, wherein step (E) further comprises:

allowing optimum results to be obtained automatically.